Seyed Hadi Mirfarshbafan

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Cornell University, Cornell Tech Campus, New York, NY

Education

Cornell University (Cornell Tech Campus) **New York, NY**
PhD student in Electrical and Computer Engineering (ECE) *2019–2020*
Advisor: Prof. Christoph Studer

Cornell University **Ithaca, NY**
PhD student in Electrical and Computer Engineering (ECE) *2018–2019*
Advisor: Prof. Christoph Studer

Sharif University of Technology **Tehran, Iran**
MSc. in Electrical Engineering, GPA: ***17.98/20*** *via 30 credits* *2016–2018*
Master Thesis: Design and Implementation of Baseband Processing Algorithms for Massive MIMO Systems
Advisor: Prof. Mahdi Shabany

Sharif University of Technology **Tehran, Iran**
BSc. in Electrical Engineering, GPA: ***18.13/20*** *via 143 credits* *2012–2016*
Undergraduate Thesis: Design and Implementation of Image Processing for Automatic Optical Inspection (AOI) systems used in detecting defects in high density PCB assembly
Thesis Advisor: Prof. Mohammad Reza Pakravan

Research Interests

- Design and implementation of algorithms and VLSI architectures for wireless communications

Industrial Work Experience

- **KavoshCom Asia Company** Tehran, Iran
  Member of Technical Staff *Jul. 2016 - Sep. 2016*

Selected Projects

- **VLSI design and implementation of high-throughput equalization** *Spring 2020*
  We designed and implemented a matrix-vector product engine capable of processing one vector per clock cycle. We created an automatic parameterized Verilog code generator in Matlab. The design was implemented on an educational 45 nm process.
- **VLSI design and implementation of Streaming MultiplierLess (SMUL) FFT engine** *Fall 2019*
  We developed an efficient multiplierless VLSI architecture for the FFT algorithm, suitable for extremely high-throughput applications, such as beamspace processing in massive MU-MIMO mmWave systems with large bandwidths. The Verilog code is generated automatically in Matlab and the VLSI design was implemented on an educational 45 nm process.
- **Near-ML Detector for Massive MIMO-OFDM systems with one-bit ADCs** *Spring 2019*
  Extended the previously proposed one-bit near maximum likelihood (ML) 1-bit detector, to massive MIMO-OFDM systems. A low-complexity VLSI architecture was also developed for the proposed algorithm.
- **Algorithm and VLSI design for beamspace channel estimation for Massive MIMO mmWave systems** *Fall 2018*

- **Near-ML Detector for Massive MIMO systems with one-bit ADCs** *Fall 2017*
  A modified near-ML detection algorithm was proposed for massive MIMO systems with one-bit ADCs. Also the corresponding low-complexity VLSI architecture was developed and implemented on Xilinx Virtex 7 FPGA, under supervision of Prof. Shabany.
- **VLSI design of ZF Precoder for Massive MIMO Systems** *Winter 2016*
  A low-complexity formulation for ZF precoder as well as a corresponding high-throughput VLSI architecture was presented that achieved a throughput of 1.1 Gbps for a system with 64 base station antennas and 8 users, under supervision of Prof. Shabany.
- Simulation, layout and post-layout simulation of a **32-bit Carry-Skip Adder**, course project for *VLSI Systems Design*
- **WiFi indoor channel model of the CE department:** We gathered field measurements of the WiFi signal RSSI and obtained a multi-wall path-loss model for the test environment, by analyzing the data in Matlab, in order to identify the optimal AP locations, course project for *Mobile Communications*
- Launching a serial JPEG camera for the ARM-based KVL300 board as the **internship task in Kavosh-Com Asia Co.,** under Supervision of Prof. Fotowat-Ahmadi
- Design and FPGA implementation of an **out-of-order 4-way superscalar pipelined 32 bits MIPS** processor, course project for *Advanced Computer Architecture*
- Design and implementation of a **Real-Time Bitmap to JPEG Compression Engine** on Xilinx Virtex 6 FPGA with a focus on maximizing throughput while keeping the area low, as well as complete ASIC design flow (floorplanning, placement and routing, layout), course project for *FPGA/ASIC Systems Design*
- **Audio record and play system showing audio waveform on LCD module** plus reading from USB flash drive on *LPC 1768* ARM training board, course project for *Microprocessor Systems Design*
- Implementation of a *real-time* **audio recognition system** on Altera's DE2 FPGA board using NIOS II processor and a custom FFT accelerator, course final project for *Microprocessor Systems Lab*
- Developing a **UDP-based communication protocol between two Android clients** with the guarantee of delivery, ordering and duplicate protection, course final project for *Data Communication Networks*
- Design and implementation of a **line follower robot** using AVR

Publications

1. S. H. Mirfarshbafan, M. Shabany, S. A. Nezamalhosseini and C. Studer, "Algorithm and VLSI Design for 1-bit Data Detection in Massive MIMO-OFDM," submitted to IEEE Open Journal of Circuits and Systems (OJCAS), May 2020
2. Z. M. Enciso, S. H. Mirfarshbafan, O. Castañeda, C. JS. Schaefer, C. Studer, and S. Joshi, "Analog vs. Digital Spatial Transforms: A Throughput, Power, and Area Comparison," 63rd IEEE International Midwest Symposium on Circuits and Systems, May 2020, *to appear*
3. S. H. Mirfarshbafan, and C. Studer, "Sparse Beamspace Equalization for Massive MU-MIMO mmWave Systems," 45th International Conference on Acoustics, Speech, and Signal Processing (ICASSP), May 2020, *to appear*
4. S. H. Mirfarshbafan, A. Gallyas-Sanhueza, R. Ghods and C. Studer, "Beamspace Channel Estimation for Massive MIMO mmWave Systems: Algorithm and VLSI Design," Oct. 2019. [Online]. Available: https://arxiv.org/abs/1910.00756
5. R. Ghods, A. Gallyas-Sanhueza, S. H. Mirfarshbafan, and C. Studer, "BEACHES: Beamspace channel estimation for multi-antenna mmWave systems and beyond," in Proc. IEEE Int. Workshop Signal Process. Advances Wireless Commun. (SPAWC), Jul. 2019
6. S. H. Mirfarshbafan, M. Shabany, A. Amini and S. A. Nezamalhosseini, "Near-ML Detection in Massive MIMO Systems with One-Bit ADCs: Algorithm and VLSI Design," 2018 IEEE International Symposium on Circuits and Systems (ISCAS), May 2018

7. S. H. Mirfarshbafan, M. Shabany, S. A. Nezamalhosseini and M. J. Emadi, "A high-throughput low-complexity VLSI architecture for ZF precoding in massive MIMO," 2017 IEEE 22nd International Workshop on Computer Aided Modeling and Design of Communication Links and Networks (CAMAD), Jul. 2017

Patents

- S. H. Mirfarshbafan, A. Gallyas-Sanhueza, R. Ghods and C. Studer, "Circuit and Method for Enabling Channel Denoising in a Wireless Communication Apparatus," Cornell University, US Patent No. 10608686, March 2020

Awards & Honors

Recipient of Jacobs Scholar Fellowship for PhD in Cornell University ..... *Fall 2018*
Offer of admission for PhD in Electrical Engineering from Rice University ..... *Fall 2018*
Offer of admission for PhD in Electrical Engineering from Columbia University ..... *Fall 2016*
Offer of admission for PhD in Electrical Engineering from Rice University ..... *Fall 2016*
Admitted to the MSc program in Electrical Engineering in Sharif University of Technology without Konkour Exam (Offered to top undergraduate students) ..... *Fall 2016*
Ranked 4th out of 25 in the class of 2014 major of digital systems *2015*
Silver Medal in Iran's National Mathematics Olympiad *2011*
Ranked 721st in Iran's university entrance exam among more than 260,000 participants of Mathematics and Technology from all across the nation *2012*

Teaching Experience

- Teaching assistant for the *Applied Digital ASIC Design* (ECE5746) course, Prof. Studer *Fall 2019*
- Teaching assistant for Cornell CATALYST academy outreach program, Prof. Studer *Summer 2019*
- Teaching assistant for the *communication systems* course, Prof. Pakravan *Fall 2016*
- Lab assistant (lab experiment designer) for the *microprocessor systems lab*, Prof. Hashemi *Fall 2016*
- Lab assistant for the *microprocessor systems lab*, Prof. Hashemi *Spring 2017, Fall 2017*
- Math Olympiad teacher for accepted students of the first round, *Shahid Madani* and *Misagh* High schools, *Tabriz* *Winter 2011, Spring 2012 & 2013*
- Iran's National Mathematics Olympiad, geometry problem grader *Spring 2013*

Skills

- **Softwares and Programming**
  - Expert:
    - **Verilog HDL**
    - **Digital ASIC design**: ModelSim, Synopsys Design Compiler, Cadence Innovus
    - **FPGA Implementation**: Xilinx ISE/Vivado
    - **ARM** and **AVR** programming
    - **C/C++**, **Assembly**(x86) and **MATLAB** programming
    - **Digital IC design with Cadence Virtuoso** (Simulation, Layout and Extraction)
  - Intermediate: **SPICE** (Pspice and Hspice), **Altium Designer**, **Simulink**, **Java**, **Python**, **CUDA**

Paper reviews

- Reviewed papers for IEEE International Symposium on Circuits and Systems (ISCAS), 2020
- Reviewed papers for 21st IEEE international workshop on Signal Processing Advances in Wireless Communications (SPAWC), 2020
- Reviewed papers for IEEE Open Journal of Circuits and Systems (OJCAS), 2020

Related Courses

Cornell University

Course Name:	**Instructor:**	**Final Grade:**
Applied Machine Learning	Prof. Belongie	B+
Digital VLSI Design	Prof. Studer	A
Digital Communications	Prof. Studer	A+

Sharif University of Technology

Course Name:	**Instructor:**	**Final Grade (out of 20):**
Digital VSLI Architectures	Prof. Shabany	17.1
FPGA/ASIC Systems Design	Prof. Shabany	18.5
Digital Electronics	Prof. Sharifkhani	20
Advanced Computer Architecture	Prof. Movahhedin	18
Mobile Communications	Prof. Khalaj	20
Matrix Computations (Math Dept.)	Prof. Mahdavi Amiri	17
Parallel Programming and Architectures	Prof. Hashemi	19.4
Microprocessor Systems Design	Prof. Sanaei	17.8
Digital Signal Processing	Prof. Mashhadi	18
Signals and Systems	Prof. Khalaj	19.1
Communication Systems	Prof. Pakravan	17.5
Analog Circuits (Electronics I)	Prof. Khorasani	20
Principles of Electronics (Electronics II)	Prof. Kavevash	18.7
Computer and Microprocessor Architecture	Prof. Jahed	18
Advanced Programming	Prof. Hashemi	19.4
FPGA-based Embedded Systems Design	Prof. Alizadeh	17.9
Computer Interfacing Circuits	Prof. Movahhedin	19