ATABERK OLGUN

https://ataberkolgun.com olgunataberk@gmail.com Google Scholar (8gmi4H0AAAAJ)

RESEARCH INTERESTS

I am interested in the intersection between **computer architecture** and memory system **reliability** and **performance**, including:

- Understanding the various properties of *read disturbance in DRAM* under different conditions and access patterns.
- Developing effective, high-performance, low-cost solutions that comprehensively mitigate read disturbance in DRAM.
- Uncovering new computational functionality in real DRAM chips to enable low-cost processing-in-memory architectures.

EDUCATION

ETH Zürich, Zürich, Switzerland 2022-Ongoing

Ph.D., Computer Engineering (adviser: Onur Mutlu)

TOBB University of Economics and Technology, Ankara, Türkiye (GPA: 4.00/4.00) 2019-2021

M.S. in Computer Engineering (adviser: Oğuz Ergin)

Thesis: "High Throughput True Random Number Generation Using Quadruple Row Activation in Real DRAM Chips." (PDF)

TOBB University of Economics and Technology, Ankara, Türkiye (GPA: 3.86/4.00) 2015-2019

B.S. in Computer Engineering (adviser: Oğuz Ergin)

HONORS & AWARDS

Best Paper Award, HiPEAC (Int'l Conference on High Performance Embedded Architecture and Compilation) 2023

Intel Hardware Security Academic Award Finalist 2022

Best Paper Award, MICRO (IEEE/ACM Int'l Symposium on Microarchitecture) 2022

FIRST AUTHOR PUBLICATIONS

1. H. Hassan*, Ataberk Olgun*, H. Luo, A. G. Yaglikci, and O. Mutlu.
   "Self-Managing DRAM: A Low-Cost Framework for Enabling Autonomous and Efficient DRAM Maintenance Operations"
   To appear in *the 57th IEEE/ACM International Symposium on Microarchitecture (MICRO-57)*, Nov. 2024.
   Open source code: https://github.com/CMU-SAFARI/SelfManagingDRAM
   *Co-primary authors

2. Ataberk Olgun, Y. C. Tugrul, N. Bostanci, I. E. Yuksel, H. Luo, S. Rhyner, A. G. Yaglikci, G. F. Oliveira, and O. Mutlu.
   "ABACuS: All-Bank Activation Counters for Scalable and Low Overhead RowHammer Mitigation."
   The 33rd USENIX Security Symposium (USENIX Sec'24), Aug. 2024.
   Open source code: https://github.com/CMU-SAFARI/ABACuS
   Officially artifact evaluated as available, functional, and reproduced.

3. Ataberk Olgun, N. Bostanci, G. F. Oliveira, Y. C. Tugrul, R. Bera, A. G. Yaglikci, H. Hassan, O. Ergin, and O. Mutlu.
   "Sectored DRAM: An Energy-Efficient High-Throughput and Practical Fine-Grained DRAM Architecture."
   ACM Transactions on Architecture and Code Optimization (ACM TACO), Jun. 2024.

4. Ataberk Olgun, M. Osseiran, Y. C. Tuğrul, H. Luo, S. Rhyner, B. Salami, J. G. Luna, and O. Mutlu.
   "Read Disturbance in High Bandwidth Memory: A Detailed Experimental Study on HBM2 DRAM Chips."
   IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-54), Jun. 2024
   Open source code: https://github.com/CMU-SAFARI/hbm-read-disturbance
   Officially artifact evaluated as available, functional, and reproduced.

5. Ataberk Olgun, M. Osseiran, Y. C. Tuğrul, H. Luo, S. Rhyner, B. Salami, J. G. Luna, and O. Mutlu.
   "An Experimental Analysis of RowHammer in HBM2 DRAM Chips."
   IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-53) – Disrupt Track, Jun. 2023

6. Ataberk Olgun, H. Hassan, A. G. Yaglikci, Y. C. Tugrul, L. Orosa, H. Luo, M. Patel, O. Ergin, and O. Mutlu.
"DRAM Bender: An Extensible and Versatile FPGA-based Infrastructure to Easily Test State-of-the-art DRAM Chips."
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), Jun. 2023.
Open source code: https://github.com/CMU-SAFARI/DRAM-Bender

7. Ataberk Olgun, J. G. Luna, K. Kanellopoulos, B. Salami, H. Hassan, O. Ergin, and O. Mutlu.
"PiDRAM: A Holistic End-to-end FPGA-based Framework for Processing-in-DRAM."
ACM Transactions on Architecture and Code Optimization (ACM TACO), March 2023.
Open source code: https://github.com/CMU-SAFARI/PiDRAM

8. Ataberk Olgun, M. Patel, A. G. Yaglikci, H. Luo, J. S. Kim, N. Bostanci, N. Vijaykumar, O. Ergin, and O. Mutlu.
"QUAC-TRNG: High-Throughput True Random Number Generation Using Quadruple Row Activation in Commodity DRAM Chips."
International Symposium on Computer Architecture (ISCA-47), May 2020.
Open source code: https://github.com/CMU-SAFARI/QUAC-TRNG

TEACHING EXPERIENCE

Digital Design and Computer Architecture (MS Level), ETH Zürich, *Lecturer*	Spring 2024
Computer Architecture (MS Level), ETH Zürich, *Lecturer*	Fall 2023
FPGA-based Exploration of DRAM and RowHammer (BS Level), ETH Zürich, *Lecturer*	2022-2024
Digital Design and Computer Architecture (BS Level), ETH Zürich, *Teaching Assistant*	2022-2024
Computer Architecture (MS Level), ETH Zürich, *Teaching Assistant*	2022-2023
Seminar in Computer Architecture (BS Level), ETH Zürich, *Teaching Assistant*	2022-2024
Computer Architecture and Organization (BS Level), TOBB ETÜ, *Teaching Assistant*	2019-2021
Digital Design (BS Level), TOBB ETÜ, *Teaching Assistant*	2019-2021
Data Communication and Computer Networks (BS Level), TOBB ETÜ, *Teaching Assistant*	2020

STUDENT MENTORSHIP

ETH Zürich Undergraduate Students: Maria Makeenkova (2022-), Steve Rhyner (2022-)

Other Students: Oguzhan Canpolat (MS, TOBB ETÜ, 2022-), Ethan Luan (BS, University of Toronto, 2023-2024)
Majd Osseiran (BS, American University of Beirut, 2022-2023)

SERVICE

- *Student assistant to the PC Chairs* for Int'l. Conf. on Dependable Systems and Networks (DSN) 2023
- *Technical Reviewer for Conferences:* ISCA, MICRO, DSN, ASPLOS, DAC, ICS
- *Technical Reviewer for Journals:* IEEE MICRO Top Picks, ACM Transactions on Embedded Computing Systems (TECS), IEEE Transactions on Circuits and Systems (TCAS), Microelectronics Reliability
- *IT Infrastructure Lead*, SAFARI Research Group, ETH Zürich, 2022-