DANILO CAMMARATA

PhD Student

Born 12/02/2001 in Turin (Italy)

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EDUCATION

Doctorate in Digital Circuits and Systems

Eidgenössische Technische Hochschule Zürich
01/10/2024 – Current
Integrated System Laboratory
PULP Platform

Master of Science MSc in Electrical and Electronics Engineering

École Polytechnique Fédérale de Lausanne
20/09/2022 – 13/06/2024
Specialization in Microelectronics

Bachelor's Degree in Electronic Engineering

Politecnico di Torino
25/09/2019 – 28/07/2022
Final Grade: 110/110 with honours

ABOUT ME

I am passionate about **knowledge** and **football**.

My love for learning has driven me to excel academically, **winning the school math challenges** six times consecutively. A fascination with the power of **computing systems** led me to study **electronics** to better understand the **hardware** operation and design, and the growing interest has convinced me to pursue this avenue for my professional career.

As for football, my leadership and teamwork skills have been recognized by my teammates and coaches, leading to my appointment as **team captain** for six years, where we reached the regional finals.

WORK EXPERIENCE

Digital IC Design Engineer Intern

Infineon Technologies AG, Dresden(Germany)
01/07/2023 – 31/12/2023
Serial Communication interfaces design from specifications to synthesis.
40hrs/week

Hardware Engineer Intern

TEST Srl, Turin(Italy)
04/10/2021 – 07/12/2021
PCB design for automotive applications, from commercial requirements to Gerber files. 40hrs/week

HARD SKILLS

Programming Languages (*C/C++/Python*)
Script Languages
HDLs (*Verilog/System Verilog/VHDL*)
OS (*Linux/Windows*)
EDA Tools (*Cadence/Synopsys/Quartus/Altium*)
Git

LANGUAGE SKILLS

Italian Native User
English C1 - Proficient User
French A2 - Basic User

PROJECTS and AWARDS

Master Project

Embedded System Laboratory, Lausanne(Switzerland)
22/01/2024 – 24/05/2024
X-HEEP Matrix Accelerator: design, verification, and integration of a systolic-array RISC-V co-processor for edge-computing SoCs.

Semester Project

Embedded System Laboratory, Lausanne(Switzerland)
20/02/2023 – 15/07/2023
Design and exploration of the Data Packing Unit for SoftSIMD micro-architecture.

Young Talent Project Award

Politecnico di Torino
29/07/2022
Extra academic activities in several domains.